Build manual modular transmitter: pll

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2020-12-11

Abstract

I obtained my ham radio licence more than twenty years ago and until recently, I had never build a radio transmitter. Starting with this document, I will publish a series of articles about the design and build of a modular radio transmitter, using mostly discrete components. The first module I have designed is a phase/frequency detector and a loop filter, which will be part of the PLL.

1 PLL 101

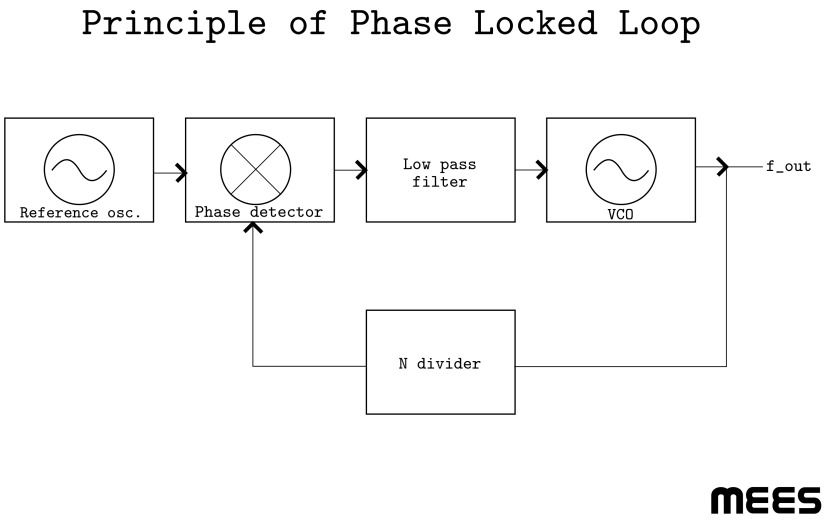

Figure 1: block diagram of a PLL

Figure 1 shows the principle of a PLL. A reference oscillator generates a signal with a stable frequency. The phase detector compares this signal with the signal from the VCO and produces an error signal which is proportional to the phase difference. This signal is fed trough a low pass filter to the VCO. A

VCO is a Voltage Controlled Oscillator. The output signal of the VCO goes through an optional divider back to the phase detector. This forms a negative feedback loop. If the output phase drifts, the error signal will increase, driving the VCO phase in the opposite direction so as to reduce the error. Thus the output phase is locked to the phase of the other input.

When the output of the VCO is divided by, lets say 10, the output frequency of the VCO will increase to 10 times the reference frequency. So by altering the divider, the frequency of the VCO can be adjusted, while still having the advantage of inheriting the stability of the reference oscillator.

2 In-depth analysis

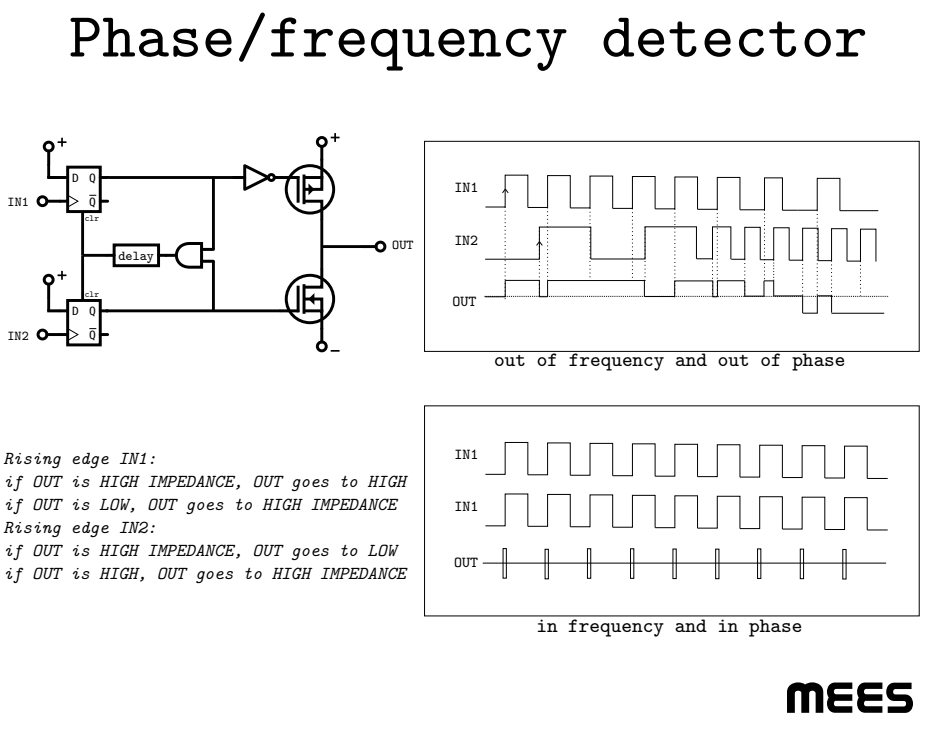

Figure 2: phase-frequency detector

For the PLL, I am going to use a phase-frequency detector, as shown in figure 2, which is build with two edge-triggered flip-flops. *IN1* and *IN2* are both input signals.

At he positive going edge of *IN1*, the output of the uppermost flip-flop switches to *HIGH* and the corresponding FET is switched on. *OUT* goes *HIGH*. At he positive going edge of *IN2*, the output of the lower flip-flop switches to *HIGH* and the corresponding FET is switched on. *OUT* goes *LOW*. This can only happen when the output of the uppermost flip-flop is not *HIGH* as well. If it is *HIGH*, the NAND gate will generate a reset-pulse and both flip-flop outputs become *LOW*. The FETs switch both off and *OUT* becomes *High Impedance*. The same is true for a positive going edge on *IN1*. When the lower flip-flop is

already *HIGH*, both flip-flops are cleared and *OUT* becomes *High Impedance*. The output *OUT* as therefore a three-state output: it can either be *HIGH*, *LOW* or *High Impedance*.

The first diagram in figure 2 shows what happens when signal *IN1* has a higher frequency than signal *IN2*: *OUT* pulses between *HIGH* and *High Impedance*. The duty-cycle is proportional to the frequency difference. When signal *IN1* has a lower frequency than signal *IN2*, *OUT* pulses between *LOW* and *High Impedance*.

Both FETs together act as a charge pump. When *OUT* is *HIGH*, a positive current can flow. When *OUT* is *LOW*, a negative current can flow. And when *OUT* is in *High Impedance* state, no current can flow.

A low pass filter, connected to *OUT*, can generate a proportion DC voltage from this pulsating signal. The DC voltage will rise when the frequency of *IN1* is higher than the frequency of *IN2*. The DC voltage will fall when the frequency of *IN1* is lower than the frequency of *IN2*. This DC voltage is the control signal for the VCO.

The second diagram in figure 2 shows what happens when both signals are phase locked to each other. On *OUT*, short pulses are present as both flip-flops are clocked simultaneously and the NAND gate resets the flip-flops almost instantaneously. The length of the pulses is determent by the delay of the three NAND gates in series. When the pulses are to short, the charge pump can stay in high impedance state for longer periods of time, therefore giving the low-pass filter the opportunity to drift. This can cause phase noise on the VCO. To prevent this, a delay is necessary.

3 Design

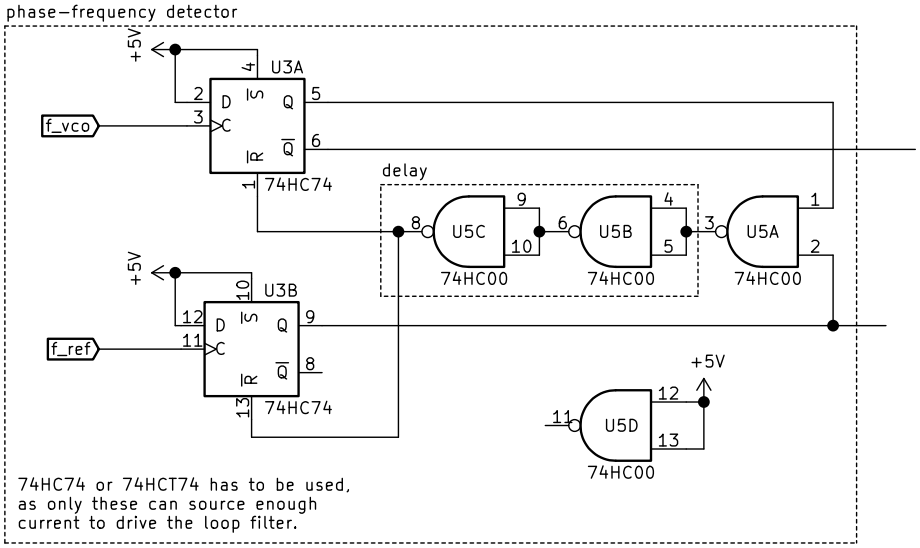

Figure 3: schematic of phase-frequency detector

In figure 3 you can see the phase-frequency detector, build around a 7474

dual flip-flop and a 7400 quad NAND gate. This part is pretty much the same as the theoretical diagram from before. The only difference is the use of a NAND gate in stead of a AND gate, because of the inverted CLEAR inputs on the flip-flops. Two extra NAND gates provide the needed delay. This way, the charge pump will still receive short pulses even when there is a perfect lock.

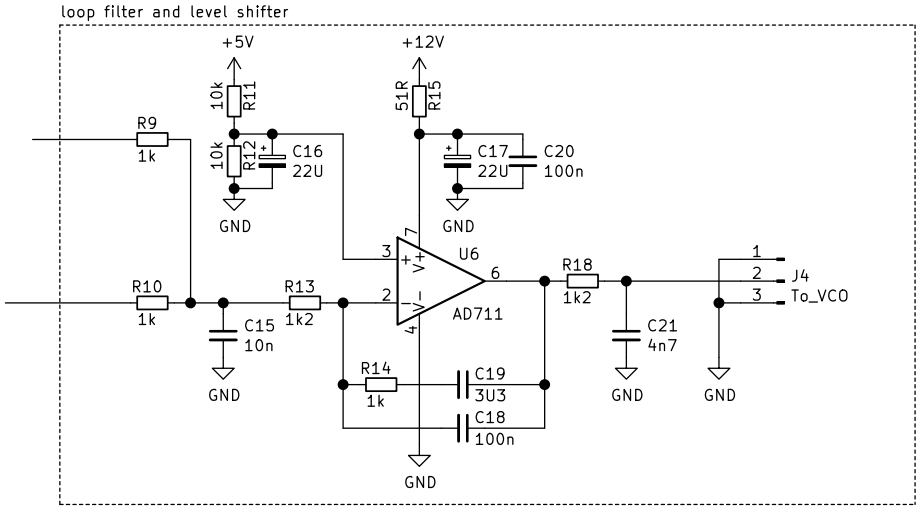

Figure 4: schematic of loop filter

In figure 4 you can see the active loop-filter, build with an AD711 opamp. Resistors R9 and R10 act as a simple charge pump.

When the frequency of the VCO drifts away from the frequency of the reference oscillator, the output of one of the flip-flops in in figure 3 goes high. Which one depends on the direction of the drift.

When the output of flip-flip U3A goes high, R9 in figure 3 is held at 0 Volts. This is because it is connected to the inverted output of the flip-flop. The output of flip-flop U3B is low, therefore R10 is also held at 0 Volt. The output of the voltage divider R9/R10, as well as the minus-input of the opamp, are now at 0 volts. The opamp is configured as an integrator and the output voltage now increases.

When the output of flip-flip U3B goes high, R10 is held at 5 Volts. The output of flip-flop U3A is low, therefore R9 is held at 5 Volt. Again, this is because it is connected to the inverted output of the flip-flop. The output of the voltage divider R9/R10, as well as the minus-input of the opamp, are now at 5 Volts. The opamp is configured as an integrator and the output voltage now decreases.

The output of the integrator is connected to a VCO, which will alter its frequency until it is the same as the frequency of the reference oscillator. When both frequencies are locked to each other, the outputs of both flip-flops will go high, causing a reset via the NAND gate, forcing the outputs to go low. Because one leg of the resistor divider R9/R10 is connected to the inverted output of flip-flop U3A and the other leg is connected to the normal output of flip-flop U3B, the output of the divider, as well as the minus-input of the opamp are now at 2.5 Vols. As this is the same voltage as is present on the plus-input of

the opamp, the system is now at rest. The opamp will no longer integrate and the output of the opamp stays at a constant voltage.

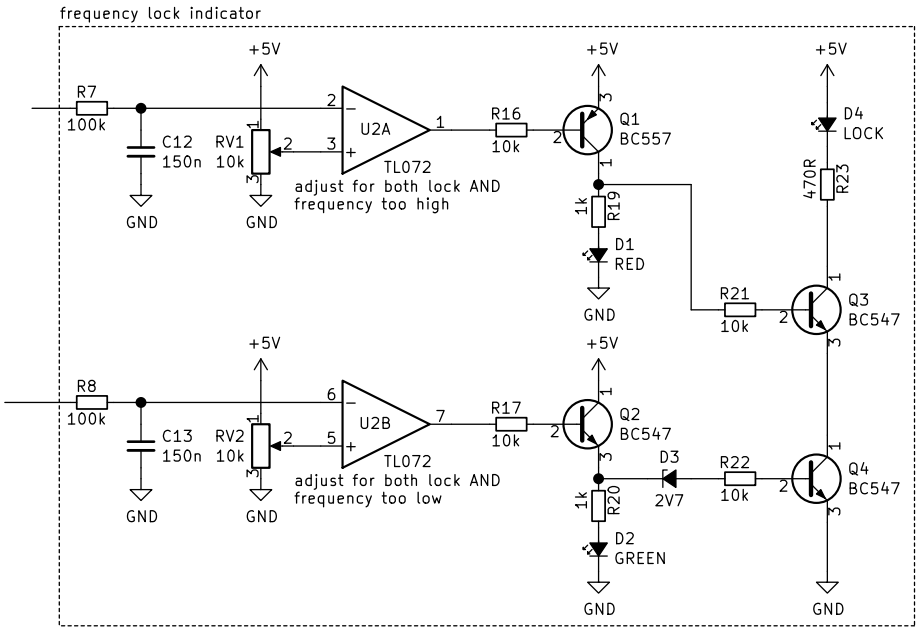

Figure 5: schematic of lock detector

In figure 5 you can see the lock detector, which light up a LED. On the outputs of both flip-flops in figure 3, short pulses are present when there is a lock. The length of the pulses is determent by the delay time of the three NAND gate in series. These pulses are very short and can easily be filtered out with a simple low pass RC-filter. The resulting DC-voltage is near zero Volts. When there is no lock, the duty-cycle of one of the flip-flop outputs will be higer and the DC-voltage after the RC-filter will rise. This can be detected by placing a comparator after each RC-filter. With potentiometers RV1 and RV2, the threshold can be set.

3.1 Testing

I tested the circuit by building the test setup as shown in figure 6. The block named PLL board is the circuit as described above, build on a breadboard. This circuit needs two power rails: a 5 Volts power supply for the digital circuitry and a 12 Volts power supply for the opamps.

A pulse generator is used as the reference oscillator. This generator has a TTL output, which can drive the phase/frequency detector.

For the VCO, I used an analog function generator with a sweep input. A DC-voltage between 0 and 10 Volts on this SWEEP input sets the frequency of the oscillator, thus making it a VCO.

Both signals are connected to an oscilloscope. The scope triggers on one signal only. Which one is not important. I am interesting in seeing a lock: this is when both signals produce stationary images on the screen. When there is

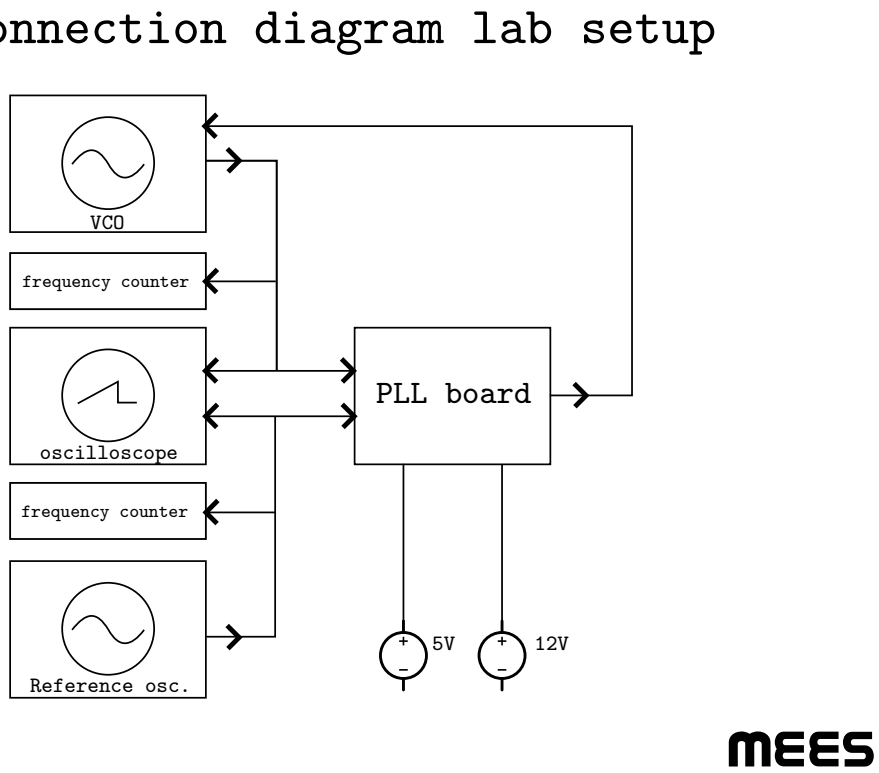

Figure 6: test setup prototype

no lock, the signal which is not used as the trigger has no relation to the other signal and will not produce a stable image.

Each signal is also connected to its own frequency counter.

The frequency of the VCO is locked to the frequency of the pulse generator. Changing the frequency of the pulse generator resultes in a change of the frequency of the VCO, just as expected. When the frequency of the pulse generator is too low or too high, the PLL cannot lock anymore. But when the frequency is changed to within the operating range of the VCO, the PLL locks again.

There was only one problem: as you can see in figure 7 there is a phase difference between both signals, but there should be none.

First, I thought it was the result of the level-shift introduced in the loop-filter (see figure 4). Changing the 2.5 Volts offset on the plus-input of the opamp altered the phase shift.

But on closer inspection, that turned out not to be the cause. The problem was the use of a 7474. This type of logic can sink current, but it cannot source current. The charge pump needs some millamps in both directions to operate. Because the system works in a closed loop, it somehow managed to lock on the frequency, by shifting the phase. The wonders of negative feedback, which make designing closed loop system both a joy and a pain at the same time. After swapping out the 7474 for a 74HC74, the system worked as intended.

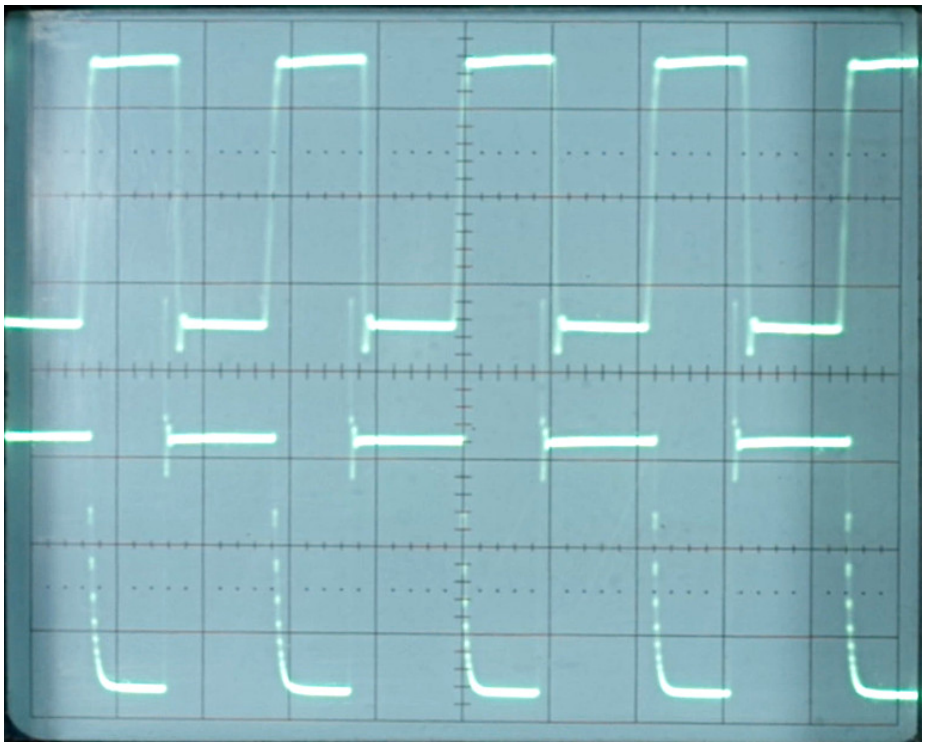

Figure 7: phase shift between reference oscillator and VCO

3.2 Clock receivers

After testing the prototype I added two clock tranceivers, as shown in figure 8. This way the PLL board can operate with input signals as low as -30 dBm. This makes the design more flexible as it can now work with a wide range of input signals, both sine wave and square wave. The input impedance is 50 Ω, set by resistors R1 and R2. NAND gates U1A and U1C are used as analog amplifiers, biased at $\frac{1}{2}$Vcc by R5 and R24. These resistors, together with R3 and R4, also set the gain.

NAND gates U1B and U1D buffer the signals, isolating the amplifiers from the phase-frequency detector.

4 Practical notes

Building the PLL board is straightforward. The design files are made with KiCad 5.1.2 and scaled PDF files of the printed circuit board are available. The pcb has only one layer and is therefore easy to make. Six wire bridges have to be soldered to the pcb. The locations of these wire bridged can be found in the appendix, figure 11.

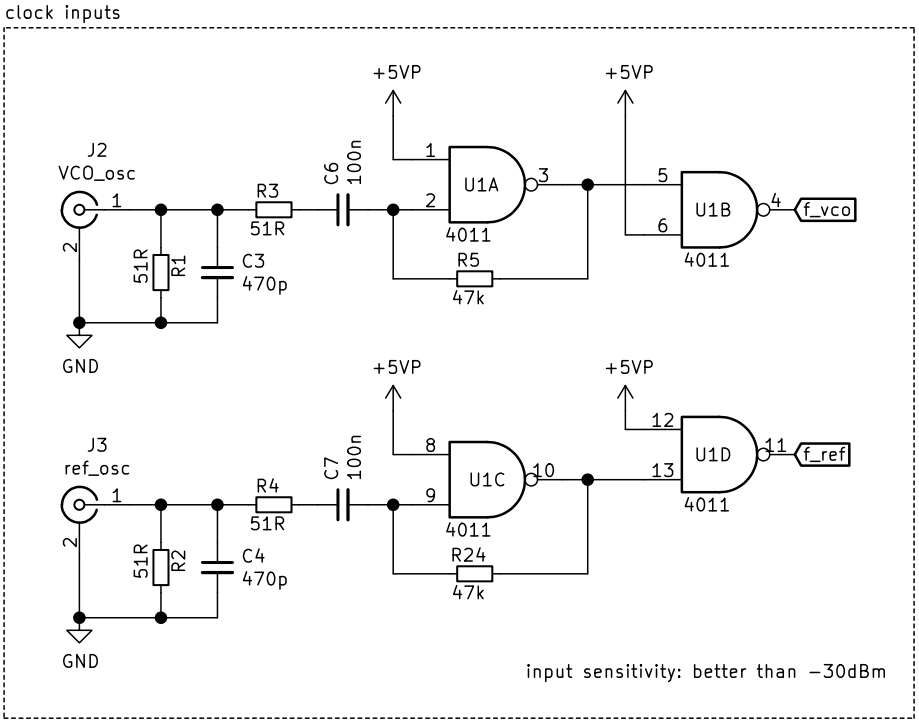

Figure 8: schematic of clock receivers

5 Adjusting lock detector

Adjust the lock detector as follows: make shure the frequency of the reference oscillator is too low for the PLL to lock. Than, adjust RV2 so that LED D2 just switches ON. Than do the same for RV1 and D1, but now with a frequency too high for a lock. The LED D4 should now only light up when there is a lock.

A Full schematic

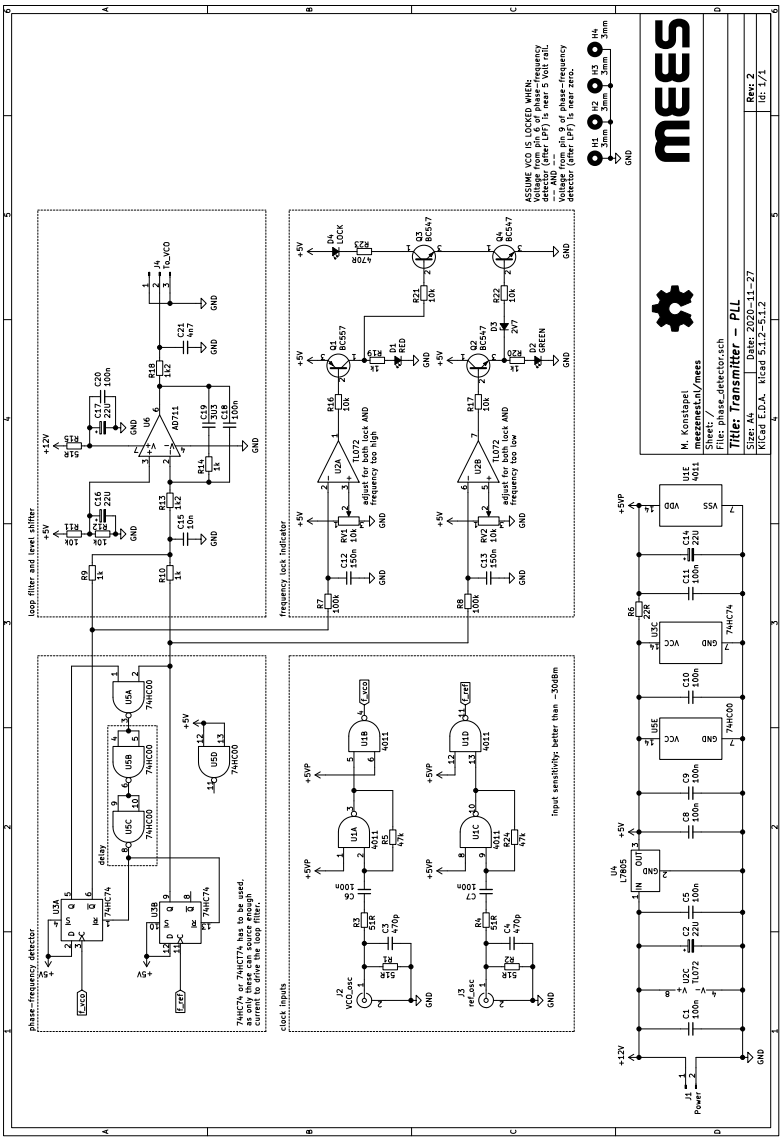

Figure 9: full schematic of PLL board

B component placement

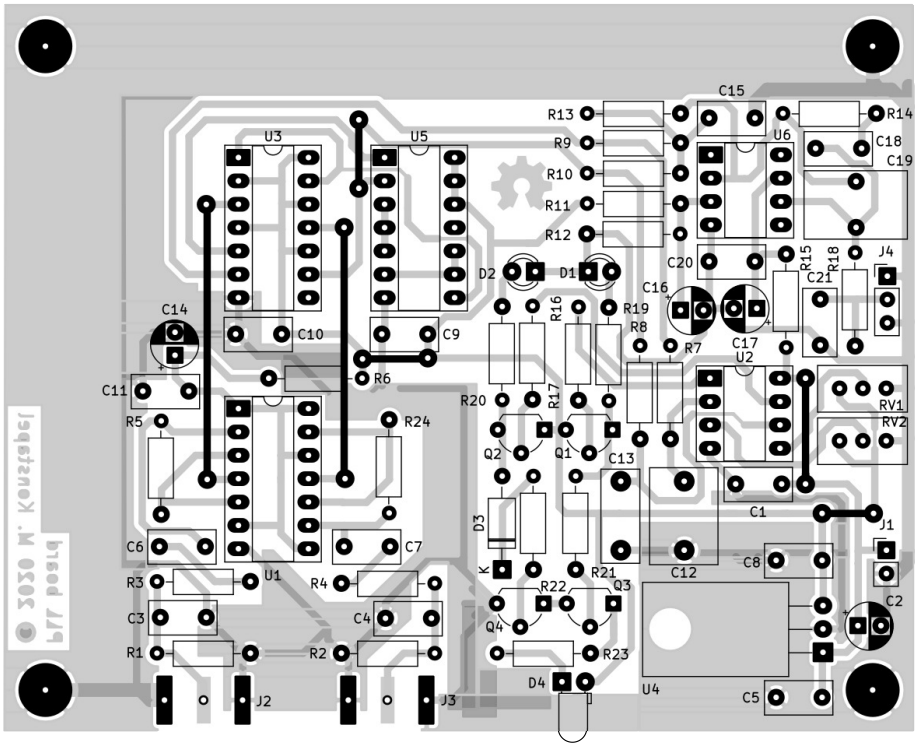

Figure 10: component placement

C Bill of material

#	References	Description	Value	Ordering #	Manufacturer
10	C1 C5 C6 C7 C8 C9 C10 C11 C18 C20	Capacitor	100n	100nF 50V 5mm pitch	QPL
1	C15	Capacitor	10n	10nF 50V 5mm pitch	QPL
1	C12	Capacitor	150n	150nF 50V 5mm pitch	QPL
1	C13	Capacitor	150n	150nF 50V 5mm pitch	QPL
4	C2 C14 C16 C17	Electrolytic capacitor	22U	22U/50V 2.5mm pitch	QPL
1	C19	Capacitor	3U3	3U3 50V foil, 5mm pitch	QPL
2	C3 C4	Capacitor	470p	470pF 50V 5mm pitch	QPL
1	C21	Capacitor	4n7	4.7nF 50V 5mm pitch	QPL
1	D3	Zener diode	2V7	2.7V 500mW	QPL
2	D1, D2	LED, orange	LED	LED orange 3mm	QPL
1	D4	LED, red	LED	LED red 3mm	QPL
1	J1	Single row connector	IDC	2 pin IDC, 2.54mm pitch	QPL
1	J4	Single row connector	SMA	3 pin IDC, 2.54mm pitch	QPL
2	J2 J3	coaxial connector SMA	SMA	leave blank	
3	Q2 Q3 Q4	Transistor NPN	BC547	BC547B	QPL
1	Q1	Transistor PNP	BC557	BC557B	QPL
2	R7 R8	Resistor	100k	100k 1% 0.25W	QPL
6	R11 R12 R16 R17 R21 R22	Resistor	10k	10k 1% 0.25W	QPL
5	R9 R10 R14 R19 R20	Resistor	1k	1k 1% 0.25W	QPL
2	R13 R18	Resistor	1k2	1k2 1% 0.25W	QPL
1	R6	Resistor	22R	22R 1% 0.25W	QPL
1	R23	Resistor	470R	470R 1% 0.25W	QPL
2	R5 R24	Resistor	47k	47k 1% 0.25W	QPL
5	R1 R2 R3 R4 R15	Resistor	51R	51R 1% 0.25W	QPL
2	RV1 RV2	Potentiometer	10k	10k multiturn	Bourns
1	U1	Quad Nand 2 inputs CMOS	HEF4011	HEF4011 DIP	QPL
1	U5	Quad Nand 2 inputs High speed CMOS	74HC00	74HC00 DIP	QPL
1	U3	Dual D Flip-flop, Set & Reset High speed CMOS	74HC74	74HC74 DIP	QPL
1	U6	Single opamp	AD711	AD711 DIP	QPL
1	U4	5 Volt regulator	LM7805	LM7805	QPL
1	U2	Dual opamp	TL072	TL072 DIP	QPL

Figure 11: bill of material